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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/656,326	09/08/2003	Hiroaki Himi	01-463	9204

23400 7590 08/09/2005

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EXAMINER	
NGUYEN, CUONG QUANG	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 08/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/656,326	HIMI ET AL.	
	Examiner	Art Unit	
	Cuong Q. Nguyen	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) *1-13,23 and 35* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14-22, 24-34, 36-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 14, 15, 20, 21, 25, 26, 27, 32, 33, 37are rejected under 35 U.S.C. 102(e) as being anticipated by Ishio et al. (US 6,653,702).

Regarding claims 14, 15, Ishio et al. discloses a method for manufacturing a semiconductor device that includes a semiconductor component (5) formed on a silicon on insulator substrate, comprising: forming a diffusion structure (11) larger than the semiconductor component in a region of the substrate in which the semiconductor component is formed; separating a part of the diffusion structure from a surrounding area thereof by trenches (14) to form the semiconductor component along with defining a size of the semiconductor component; and connecting a metallization pattern (19) to the semiconductor component. See Fig.1 and Fig.2A to Fig.2B.

Regarding claims 20-21, as shown in Ishio et al.'s Fig.1, wherein the semiconductor device (a bipolar transistor) formed in separating step is an analog component for processing an analog signal. See Ishio et al.'s col.3 lines 50-56.

Regarding claims 25, 26, 27, 32, 33, 37, as shown in Ishio et al.'s Fig.1, the semiconductor device is a hybrid IC including BJT (5) and MOSFET (6).

Claims 14, 15, 18, 19, 22, 24, 30, 31, 34, 36, are rejected under 35 U.S.C. 102(b) as being anticipated by Koyama et al. (US 2001/0032990).

Regarding claims 14, 15, Koyama et al. discloses a method for manufacturing a semiconductor device that includes semiconductor components (LDMOS device 3, 4) formed on a silicon on insulator substrate, comprising: forming a diffusion structure larger than the semiconductor component in a region of the substrate in which the semiconductor component is formed; separating a part of the diffusion structure from a surrounding area thereof by a trench structure to form the semiconductor component along with defining a size of the semiconductor component; and connecting a metallization pattern to the semiconductor component. See Fig.1 and Fig.3.

Regarding claim 18, 19, 30, 31, as shown in Koyama et al.'s Fig.2 and [0030] at right column of page 2, the diffusion structure is formed including a repeated pattern of rectangular shape in the region.

Regarding claims 22, 24, 34, 36, Koyama et al. teaches that the semiconductor device (LDMOS device) formed in separated step is a power component for controlling power supply. See [0019] at right column of page 1.

Claims 14, 17, 25, 26, 27, 29, 32, 33, 37 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamazaki (US 5,306,940).

Yamazaki discloses a method for manufacturing a semiconductor device that includes semiconductor components (BJT and MOSFET devices) formed on a substrate, comprising: forming a diffusion structure (103) larger than the semiconductor component in a region of the substrate in which the semiconductor component is formed; separating a part of the diffusion structure from a surrounding area thereof by a trench structure (112) filling with borophosphosilicate glass (BPSG 115C) (col.10 lines 64-68) to form the semiconductor component along with defining a size of the semiconductor component; and connecting a metallization pattern (131) to the semiconductor component. See Fig.8A to Fig.8H.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 16 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishio et al. and Koyama et al.

Ishio et al. And Koyama et al. do not explicitly teach that a semiconductor layer on an insulating layer is equal to or less than five microns as claimed because the thickness of the semiconductor layer would have been determinable by one of ordinary skill in the art through no more than routine experimentation and optimization. See In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955). It would have been obvious to one of ordinary skill in the art to form the semiconductor layer as thin as claimed in order to reduce the size of the semiconductor device.

Response to Arguments

3. Applicant's arguments filed 07-28-05 have been fully considered but they are not persuasive.

Applicants argue that the diffusion structure in Ishio et al. is not a diffusion structure. In response, it is clearly shown in Ishio et al.'s Fig.1 and Fig.2B that the layer (11) is an n type diffusion region which is separated by trench (14) to form a plurality of element forming regions. It is noted that the layer (11) is identical to layer (13, 14) of the present invention which is larger than the semiconductor component.

Applicants argue that there is no support for a trench is formed in Koyama et al.'s device. It is clearly shown in Koyama et al.'s Fig.3 a trench (under the LOCOS regions and adjacent to "DEEP N^+ regions) is formed in the substrate.

Applicants argue that Yamazaki fials to disclose the claimed trench. In response, it clearly shown in Yamazaki's Fig.8C, the trench structure (112) is formed in the substrate.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

5. Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 872-9306. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

6. Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to CUONG Q NGUYEN whose telephone number is (571) 272-1661. The Examiner is in the Office generally between the hours of 6:30 AM to 5:00 PM (Eastern Standard Time) Monday through Thursday.

7. If attempts to reach the examiner by telephone are unsuccessful, the Primary examiner Steven Loke who can be reached on (571) 272-1657.

Cuong Nguyen

Primary examiner

8/6/05